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An AMOLED Pixel Circuit for 1000 ppi and 5.87-inch Mobile Displays with AR and VR Applications

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Abstract

In this paper, an active-matrix organic light emitting diode (AMOLED) pixel circuit is proposed for 1000 ppi and 5.87-inch mobile displays with augmented and virtual reality applications. The proposed pixel circuit consisting of 3 thin-film transistors (TFTs) and 2 capacitors employs a simultaneous emission driving method to reduce the number of TFTs. The simulation results of the proposed pixel circuit showed that the emission current errors caused by the threshold voltage variation of driving TFT and crosstalk error were less than ±0.4 LSB and ±1 LSB, respectively, over the entire gray level. Therefore, the proposed pixel circuit is highly suitable for AMOLED displays.

Author Keywords

AMOLED, Pixel circuit of AMOLED, High-resolution display, Augmented reality, Virtual reality, Head-mounted display

1. Introduction

The organic light-emitting diode (OLED) on silicon (OLEDoS) displays have increasingly gained much attention for augmented and virtual reality (AR and VR) applications due to their high contrast ratio and fast optical response time [1, 2]. However, they have suffered from high cost because the display panels using the OLEDoS were fabricated on a silicon wafer [1, 2]. The fabrication cost of the display panels can be reduced using a glass or flexible substrate, which is generally employed for the small-area active-matrix OLED (AMOLED) displays [3-11], rather than a silicon wafer.

However, the glass and flexible substrates have the electrical characteristic variation of low-temperature poly-crystalline silicon (LTPS) thin-film transistors (TFTs) caused by irregular grain boundaries [3]. To compensate for these electrical characteristic variations, the external compensation method, luminance adjusting algorithm, and diode-connection scheme have been researched [4-12]. The external compensation method [4-7] and luminance adjusting algorithm [8] increase the system cost due to the additional logic blocks and memories for sensing the electrical characteristic variation of the driving TFTs and modulating the data voltage. Therefore, the diode-connection schemes [9-13] have been widely used for small-area AMOLED displays. To drive the AMOLED displays with diode-connection scheme, the progressive emission (PE), block emission (BE), and simultaneous emission (SE) driving methods have been used [12, 13]. The PE and BE driving methods have a long emission time, but require complex pixel circuits to control the emission current flow through OLEDs. On the other hand, the SE driving method reduces the number of TFTs by modulating the voltage of ELVDD.

In this paper, an AMOLED pixel circuit consisting of only 3 TFTs and 2 capacitors is proposed for 1000 ppi mobile displays with AR and VR applications. The proposed pixel circuit, which is designed for 5.87-inch and 5120×2880 resolution, employs the SE driving method to reduce the number of TFTs.

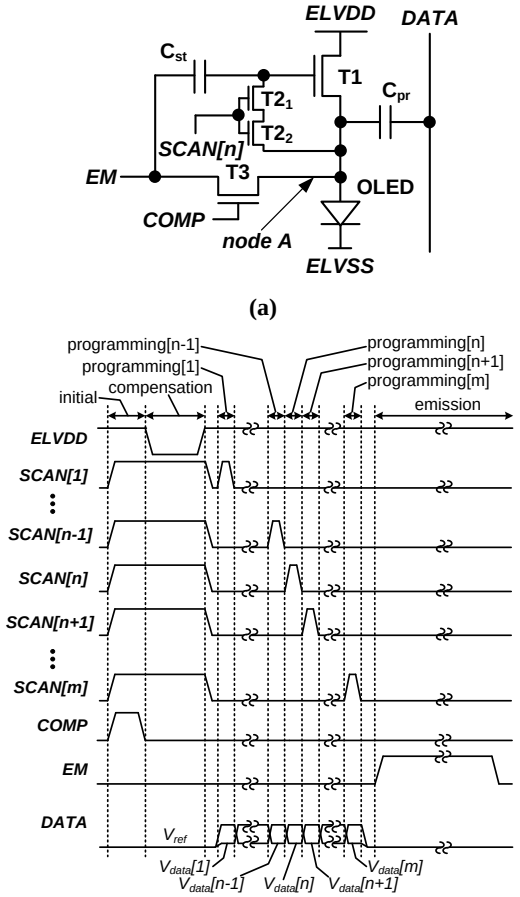

Figure 1. (a) Schematic and (b) timing diagram of the proposed pixel circuit.

2. Proposed Pixel Circuit

Figure 1(a) and (b) show the schematic and timing diagram of the proposed pixel circuit consisting of 3 TFTs and 2 capacitors. T1 is a driving TFT to supply an emission current to OLED, and T2 and T3 are switching TFTs. T2 is designed with a dual gate to reduce the voltage distortion of gate node of T1, which is caused by the leakage current through T2. The *ELVDD*, *COMP*, and *EM* signals are globally applied to all row lines in the display panel. The *SCAN[1]* to *SCAN[m]* signals, where m is the number of row lines, are individually applied to each row line. The proposed pixel circuit, which employs the SE driving method, operates in the initial, compensation, programming, and emission phases, as shown in Figure 1 (b).

In the initial phase, the *SCAN[1]* to *SCAN[m]* and *COMP* signals are high to turn on T2 and T3. Then, the gate voltage of

T1 ($V_{gate,T1}$) and the voltage at node A (V_A) are initialized to the low voltage of *EM* signal (EM_{low}). Since the gate-to-source voltage of T1 is zero while the turn-on voltage of T1 is 0.45 V, T1 is turned off, and thus the short circuit current from ELVDD to EM does not flow. In addition, since EM_{low} is less than or equal to ELVSS, the OLED is turned off.

In the compensation phase, the *SCAN[1]* to *SCAN[m]* signals maintain high to turn on T2 and the *COMP* signal becomes low to turn off T3. Also, the *ELVDD* signal becomes a low voltage ($ELVDD_{low}$), which is lower than EM_{low}. Then, $V_{gate,T1}$ decreases until it becomes $ELVDD_{low}+V_{th,T1}$, where $V_{th,T1}$ is the threshold voltage of T1. The charges stored in C_{st} (Q_{st}) and C_{pr} (Q_{pr}) can be respectively expressed as

$$Q_{st} = C_{st}\times(ELVDD_{low}+V_{th,T1}-EM_{low}) \quad (1)$$

and

$$Q_{pr} = C_{pr}\times(ELVDD_{low}+V_{th,T1}-V_{ref}), \quad (2)$$

In the programming[1] to programming[n-1] phases, the *SCAN[1]* to *SCAN[n-1]* signals are progressively applied to each row line as a pulse signal, respectively, and the charges stored in C_{st} and C_{pr} remain unchanged since the gate of T1 and the anode of the OLED are floating.

In the programming[n] phase, the *COMP* signal maintains low to turn off T3 and the *SCAN[n]* signal becomes high to turn on T2. Also, the *data* signal becomes $V_{data}[n]$. Since Q_{st} and Q_{pr} are unchanged, $V_{gate,T1}$ can be derived as (3).

$$\begin{aligned} &C_{st}(ELVDD_{low}+V_{th,T1}-EM_{low})+C_{pr}(ELVDD_{low}+V_{th,T1}-V_{ref}) \\ &=C_{st}(V_{gate,T1}-EM_{low})+C_{pr}(V_{gate,T1}-V_{data}[n]) \\ &\therefore V_{gate,T1}=ELVDD_{low}+V_{th,T1}-\frac{C_{pr}}{C_{st}+C_{pr}}\times(V_{ref}-V_{data}[n]). \end{aligned} \quad (3)$$

After the programming[n] phase, the *SCAN[n]* signal becomes low to turn off T2 and $V_{gate,T1}$ is unchanged due to C_{st} until the emission phase begins. Between the programming[1] and programming[m] phases, since the gate-to-source voltage of T1 (V_{GS}) and V_A are smaller than $V_{th,T1}$ and turn-on voltage of the OLED, respectively, the OLED doesn`t emit light. Therefore, a switch for preventing the *DATA* signal from being transferred to C_{pr} is not needed, and thus the number of TFTs can be reduced.

In the emission phase, the *EM* signal becomes a high voltage (EM_{high}) to increase $V_{gate,T1}$ to be larger than $V_{th,T1}$. Then, $V_{gate,T1}$ can be expressed as (4).

$$V_{gate,T1}=ELVDD_{low}+V_{th,T1}-\frac{C_{pr}}{C_{st}+C_{pr}}\times(V_{ref}-V_{data}[n])+\Delta EM, \quad (4)$$

where ΔEM is equal to EM_{high}-EM_{low}. Also, the emission current (I_{T1}) is expressed as (5).

$$\begin{aligned} I_{T1}&=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th,T1})^2 \\ &=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(ELVDD_{low}-\frac{C_{pr}\times(V_{ref}-V_{data}[n])}{C_{st}+C_{pr}}+\Delta EM-V_A), \end{aligned} \quad (5)$$

where μ_n, C_{ox}, and *W/L* are the mobility, the gate capacitance per unit area, and the ratio of channel width to length of T1. Therefore, I_{T1} becomes independent of variation in $V_{th,T1}$.

Table 1. Simulation conditions.

Design parameter	Value
$ELVDD_{high}$ (V)	7 V
ELVSS (V)	0 V
W/L of T1	1.6 μm/9.0 μm
W/L of switches	1.6 μm/3.5 μm
C_{st}	20 fF
C_{pr}	70 fF
Unit pixel area	12.7 μm×25.4 μm
Maximum emission current	4 nA
Target application	5.87-inch (5120×2880, pentile)

3. Simulation Results

To verify the performance of the proposed pixel circuit, the emission current error caused by $V_{th,T1}$ variation and crosstalk error of the proposed pixel circuit were simulated under the simulation conditions shown in Table 1. The emission current and crosstalk errors are expressed in LSB, which represents the gray difference. Figure 2 shows the simulated emission current error of the proposed pixel circuit, showing that the emission current error is less than ±0.4 LSB over the entire gray level when $V_{th,T1}$ variation is ±0.348 V.

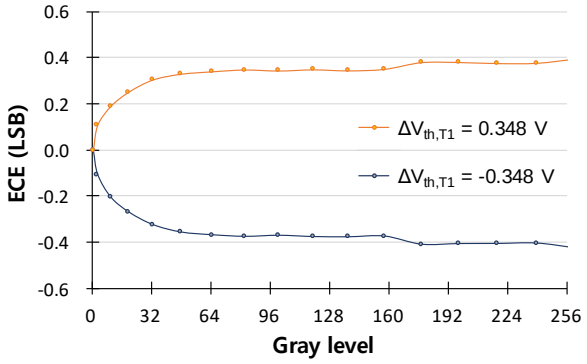

Figure 2. Emission current error according to gray level when $V_{th,T1}$ variation is ±0.348 V

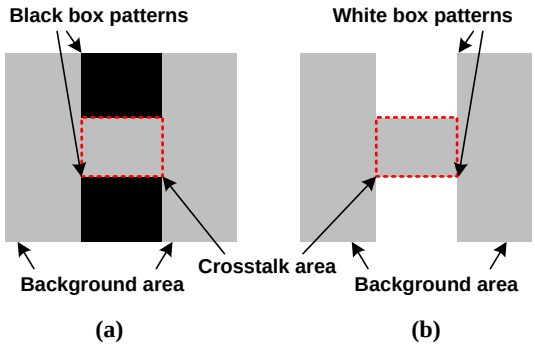

Figure 3. Input images for verifying the crosstalk error caused by leakage current through T2: with (a) black box and (b) white box patterns

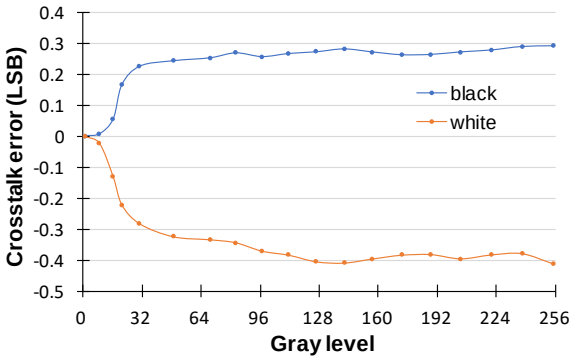

Figure 4. Crosstalk error caused by the leakage current through T1 and T2 according to the gray level

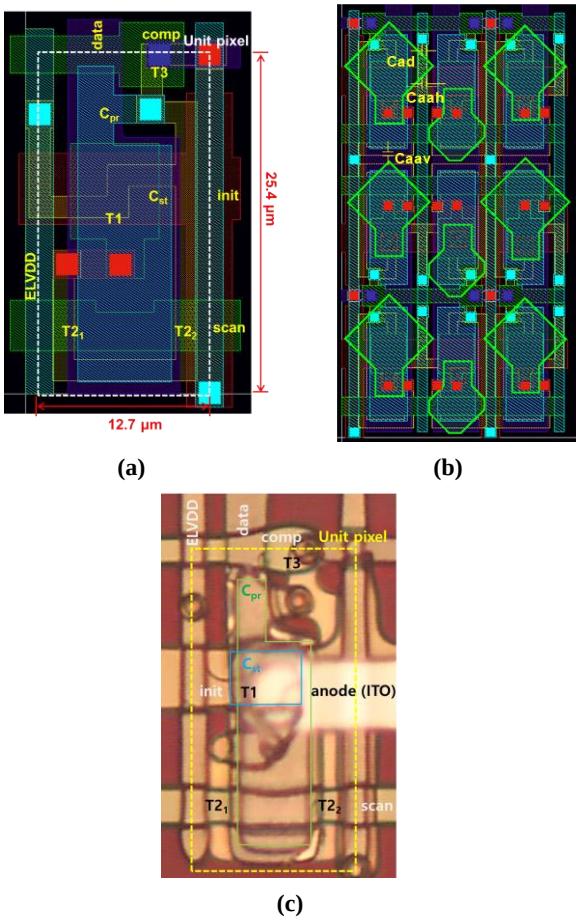

Figure 5. **(a)** Unit pixel and (b) 3x3 pixel array layouts of the proposed pixel circuit and (c) photomicrography of unit pixel

The crosstalk error caused by the leakage current of T1 and T2 were verified using the input images with the black (0^{th} gray level) box and white (255^{th} gray level) box patterns as shown in Figure 3(a) and (b), respectively. When the same data voltage for a gray level is programmed to the crosstalk and background areas, the luminance of the crosstalk area may differ from that of the background area due to the leakage current through T1 and T2.

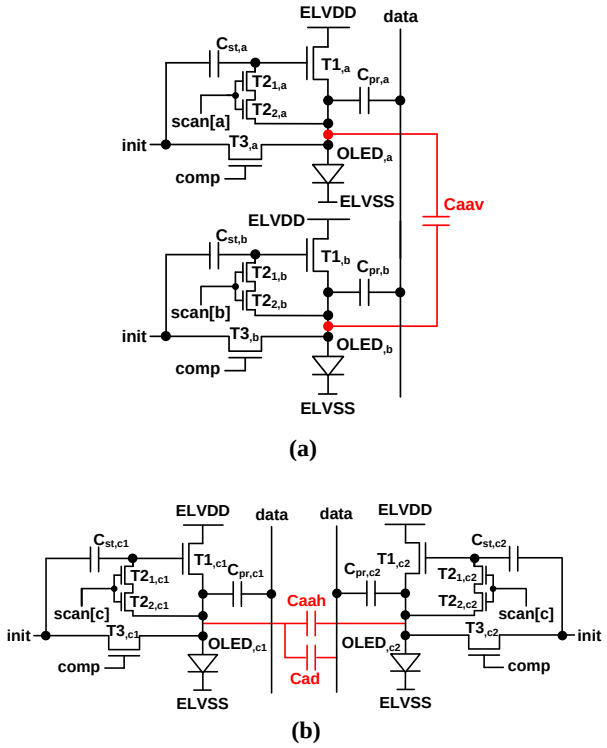

Figure 6. Schematics of (a) vertically and (b) horizontally adjacent pixel circuits

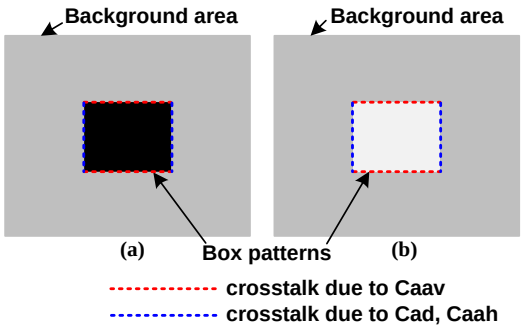

Figure 7. Input images for verifying the crosstalk error caused by Caav, Cad, and Caah: with (a) black box and (b) white box patterns

Figure 4 shows the simulated crosstalk error of the proposed pixel circuit according to the gray levels of the background and crosstalk areas, showing that the crosstalk error is less than ±1 LSB over the entire gray level.

Since the proposed pixel circuit is designed for a high spatial resolution of 1000 ppi, the parasitic capacitances between the nodes of the adjacent pixel circuits are relatively larger than those of the conventional small-area AMOLED display, and thereby may cause a larger crosstalk error. Figure 5(a), (b), and (c) respectively show the layouts of the unit pixel and 3×3 pixel array for the proposed pixel circuit and photomicrography of unit pixel. Among the parasitic capacitances, Caav, Caah, and Cad in Figure 5(b) mainly cause the crosstalk error of the proposed pixel circuit.

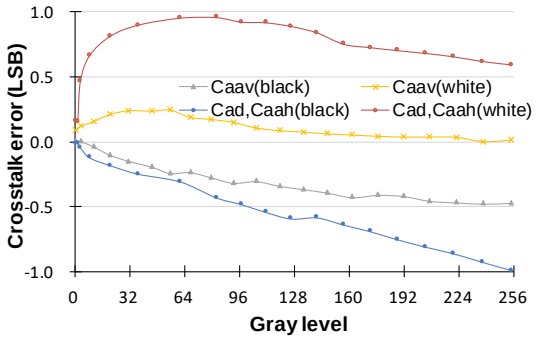

Figure 8. Crosstalk error caused by Caav, Cad, and Caah, extracted from the layout in Figure 5(b), according to the gray level

Figure 9. Demonstration of prototype panel using the proposed pixel circuit, which was captured using a camera through the magnifying glass lens in the head-mounted device

Figure 6(a) and (b) respectively show the schematics of vertically and horizontally adjacent pixel circuits including Caav (0.16fF), and Caah (0.03 fF) and Cad (0.12 fF).Figure 7(a) and (b) show the input images with black and white box patterns, respectively, for verifying the crosstalk error caused by Caav, Caah, and Cad. The crosstalk occurs at the outer border of the box patterns due to Caav, and Caah and Cad as marked in the red- and blue-dotted lines, respectively. Figure 8 shows that the crosstalk errors are less than ±1 LSB over the entire gray level. Therefore, the crosstalk errors caused by the leakage current of T1, T2, Caav, Caah and Cad would not be perceived by human eyes.

Figure 9 shows a demonstration of the prototype display panel using the proposed pixel circuit, which was designed for 5.87-inch and 5120×2880 resolution. It was captured using a camera through the magnifying glass lens in the head-mounted device.

4. Conclusion

In this paper, an AMOLED pixel circuit, which is designed for 5.87-inch and 1000 ppi mobile displays with AR and VR applications, is proposed. The proposed pixel circuit, which consists of only 3 TFTs and 2 capacitors, employs the SE driving method to reduce the number of TFTs. The simulation results of the proposed pixel circuit show that the emission current and crosstalk errors were less than ±0.4 LSB and ±1 LSB, respectively. Therefore, the proposed pixel circuit is highly suitable for AMOLED displays requiring small area and high spatial resolution.

5. References

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